Event-Driven Correlated Double Sampling for Pulse-Frequency-Modulation A/D Converters Integrated in Pixel-Parallel Image Sensors

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Abstract

We report a novel event-driven correlated double sampling (CDS) technique for pulse-frequency-modulation (PFM) analog-to-digital converters (ADCs). PFM-ADCs are promising for pixel-parallel 3-D integrated image sensors with excellent imaging performance. The developed ADC with CDS consists of comparators, capacitors, and timing control logic circuits that are designed to generate the triggered clocks to cancel kTC noise in a pixel. We confirmed that the prototype ADC showed noise reduction effects and also an excellent linearity with a wide dynamic range of 120 dB, which indicates the feasibility of high-quality pixel-wise image sensors.

Introduction

Recent demands are escalating for higher resolution and frame rate of image sensors [1]. Pixel-wise signal processing combined with 3-D integration technology is a promising solution to meet future demands. We have developed a pixel-parallel 3-D integrated image sensor as shown in Fig. 1 [2-4]. Several silicon-on-insulator (SOI) layers are bonded and connected within every pixel by high-density embedded Au electrodes [5].

We adopted PFM-ADCs [6] for the sensor, whose basic configurations are shown in Fig. 2. The ADCs generate pulses whose frequencies are proportional to the illuminance. The ADC has advantages of small footprint, wide dynamic range, and high tolerance to noise outside pixel. However, kTC noise during resetting the PD causes a deviation of pulse frequency as noise per pixel. The conventional CDS is operated to cancel the kTC noise by periodical clocks for reset, clamp, and sample [7-8]. However, such periodical signals are not available for PFM-ADCs because the reset clock is identical to the output pulse and that the timing of which is not periodic but depends on illuminance.

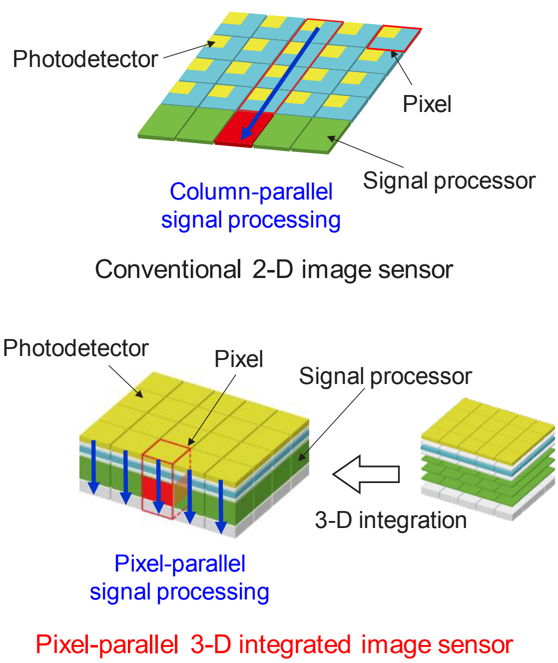


Figure 1: Pixel-parallel 3-D integrated image sensor compared with the conventional 2-D sensor.

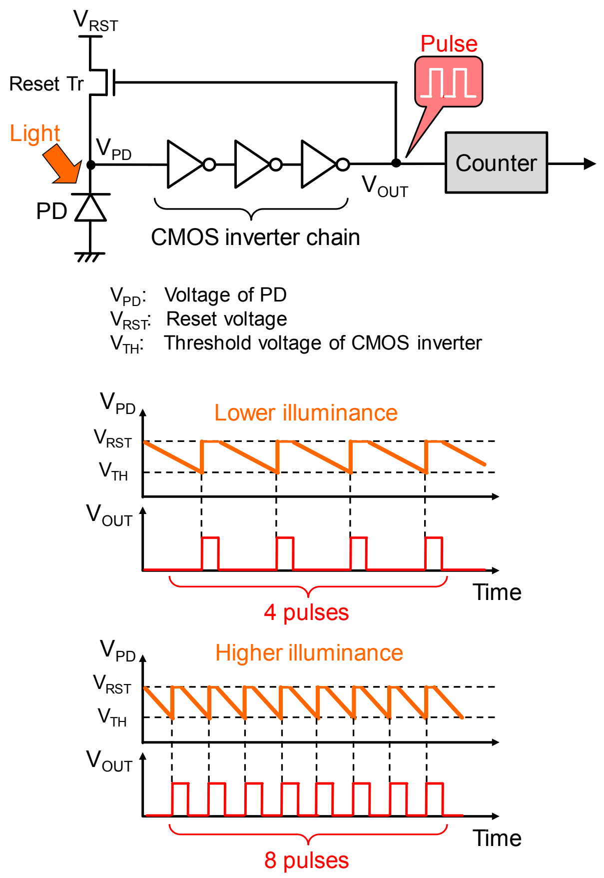


Figure 2: Circuit diagram and operation timing chart of conventional PFM-ADC.

Circuit Design

We have developed an event-driven CDS applicable to PFM-ADCs as shown in Fig. 3. The signal charge in pinned photodiode (PD) is transferred to floating diffusion (FD) connected to the clamp capacitor (C_{CP}) and the reset (RST) transistor. The comparator and inverter chain outputs pulses (P_OUT). The operation of the timing control logic circuits is as follows: the delay circuits create D1 and D2 as delayed pulses of P_OUT. The NAND, NOR, and OR circuits generate the logical product and sum of P_OUT, D1, and D2. They are applied to the RST transistor, the clamp (CP) transistor, and the signal transfer (TX) transistor for the CDS operation, where C_{CP} maintains the voltage difference (ΔV) to cancel the kTC noise. The event-driven circuits realize the noise reduction operation triggered by P_OUT in each pixel.

Fig. 4 shows simulation results of the designed ADC, where the reset voltage (V_{RST}) is 3 V, the reference voltage (V_{REF}) is 2 V, and the threshold voltage of comparator (V_{TH}) is 1.5 V. The voltages of several nodes are plotted as shown in Fig. 4 (a), where the comparator input node (C_IN) changes with tracing the FD potential (FD). P_OUT is activated whenever C_IN reaches V_{TH}. Fig. 4 (b) shows the waveforms of the timing control logic circuits. Pulse output width and delay time per stage are set as 20 ns and 6 ns, respectively. The logic circuits can generate waveforms required for the CDS operation as designed.

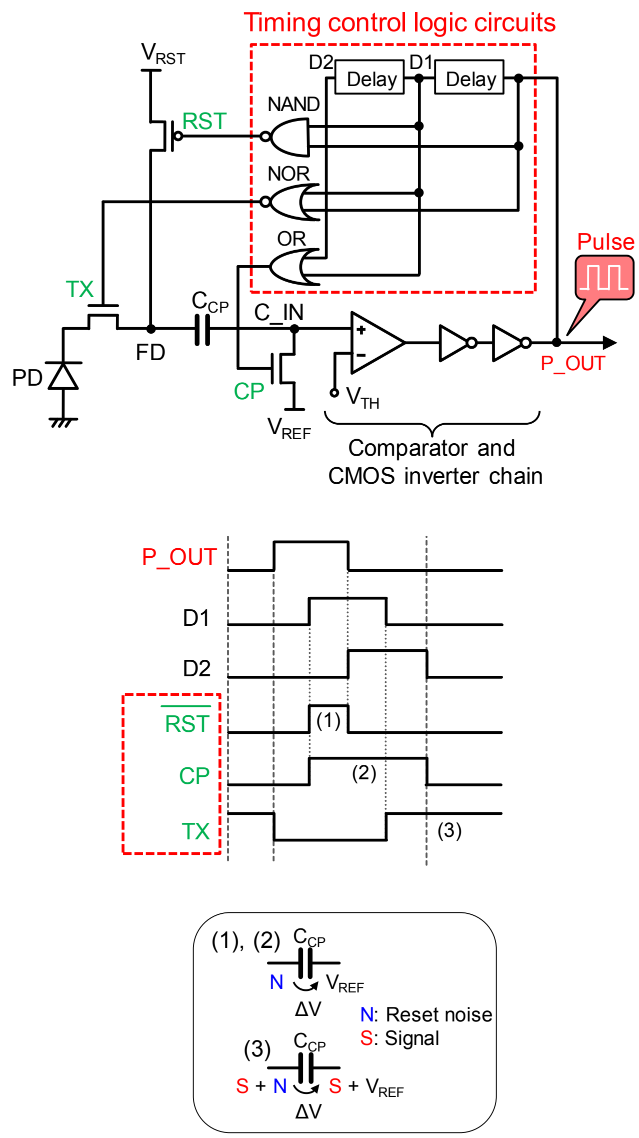
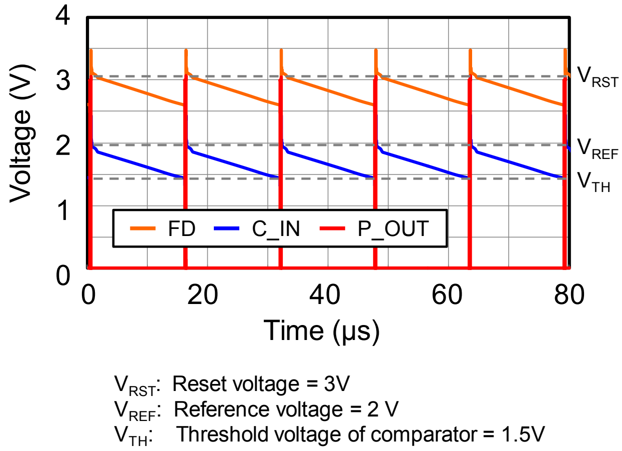
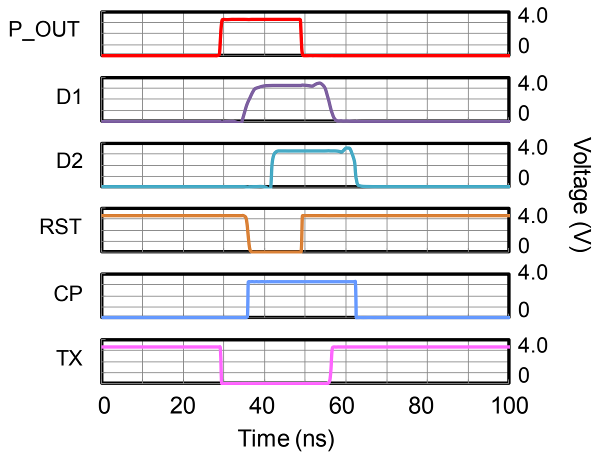


Figure 3: Schematic diagram and timing chart of the developed PFM-ADCs with event-driven CDS.



(a)



(b)

Figure 4: Simulation results for designed PFM-ADC with event-driven CDS.

Measurement Results

Fig. 5 shows chip photographs of the prototype ADCs on 3-μm-thick SOI. We obtained pulse outputs with their frequencies corresponding to the illuminance as shown in Fig. 6. Fig. 7 (a) evaluates the noise reduction effects of the ADCs with CDS by comparing them with the identical ADCs without CDS. While frequency of ADC without CDS is proportional to the reset voltage, the developed ADC with CDS suppresses the deviation to below 1%, which is caused by the fluctuations of the light-source. Fig. 7 (b) shows the input–output characteristics of the ADC with CDS, which confirms a wide dynamic range of 120 dB with an excellent linearity. We thus demonstrated the successful operation of novel PFM-ADCs with event-driven CDS.

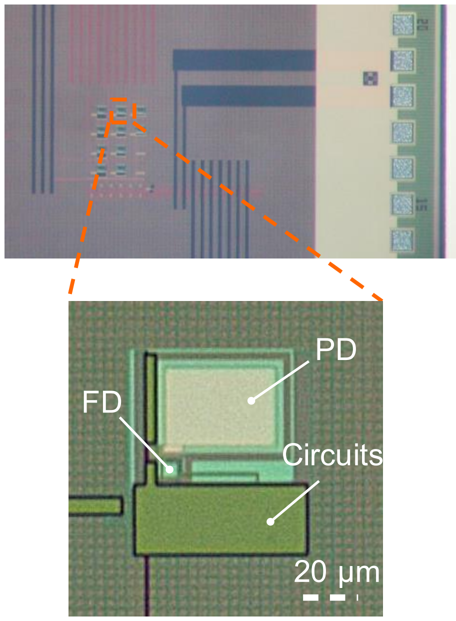


Figure 5: Chip photographs of the prototype ADCs.

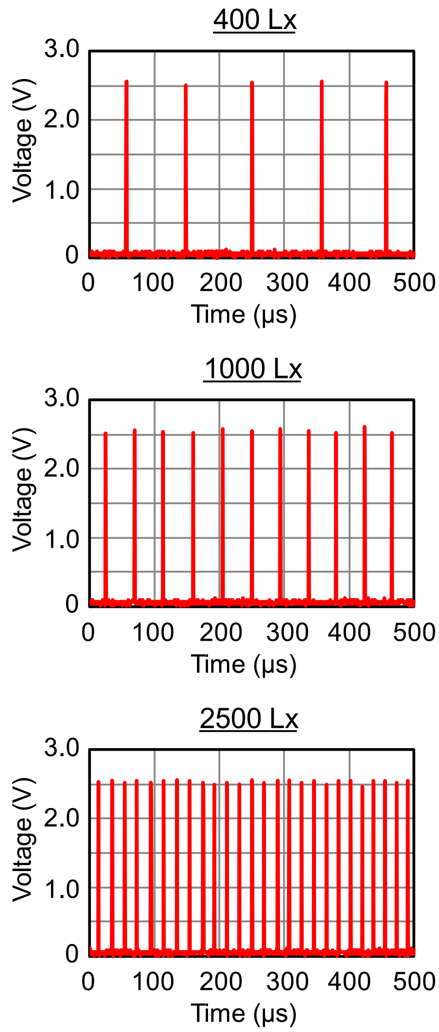


Figure 6: Measured outputs of the developed ADCs for different illuminance conditions.

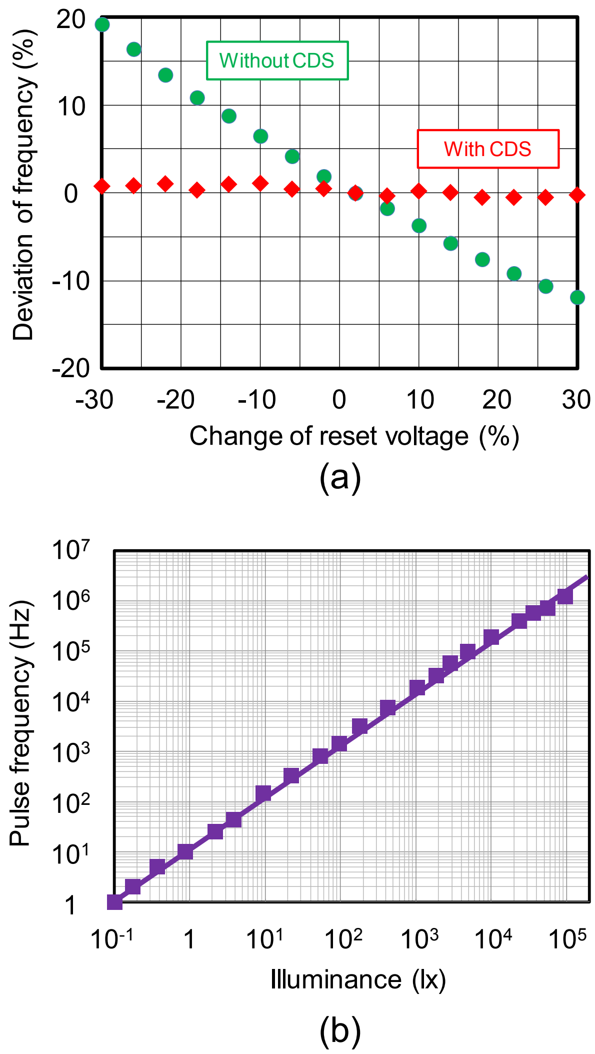


Figure 7: (a) Deviation of the pulse frequency against reset voltage change and (b) input–output characteristics.

Conclusion

We developed PFM-ADCs with a novel event-driven CDS technique. Measurement results demonstrated in-pixel noise reduction effects of below 1% and a wide dynamic range of 120 dB with an excellent linearity. The ADCs are promising for the pixel-parallel 3-D integrated image sensor with ultimate performances.

References

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